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"fringe region" "memory test" "memory cells"

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Discrete tests for weak bits

S Tandjøerg - 2005 - freepatentsonline.com

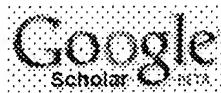
... column and row defining a memory cell in a **fringe region** of said ... [0011] Another known **memory test** is the checkerboard test, where the **memory cells** 170 of ...

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"fringe region" "memory test" "mem"

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"fringe region" "memory test"

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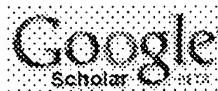
... a row of said memory array to be tested, said selected column and row defining a memory cell in a **fringe region** of said ... [0011] Another known **memory test** is the ...

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"fringe region" "memory test"

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"fringe region" "memory testing"

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Discrete tests for weak bits

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... said selected column and row defining a memory cell in a **fringe region** of said ... are thousands of word lines in one memory device, the **memory testing** takes long ...

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"fringe region" "memory testing"

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All Results

[Embedded memory testing method and apparatus - all 2 versions »](#)

RC Beauchene, RJ Russell - US Patent 4,481,627, 1984 - Google Patents

... f 4,481,627 I2 Incorporated "AS Series", produce an even greater EMBEDDED MEMORY
TESTING METHOD AND ... singled out for test. Instead of using a card-**edge** con- ...

Cited by 36 - Related Articles - Web Search

[Loss of Recent Memory After Bilateral Hippocampal Lesions - all 5 versions »](#)

WB Scoville, B Milner - 2000 - Am Neuropsych Assoc

... of the temporal lobes, with the temporal horn constituting the lateral **edge** of
resection ... Yet formal **memory testing** revealed the same deficit as that shown by AZ ...

Cited by 1248 - Related Articles - Web Search

[Tutorial on semiconductor memory testing - all 2 versions »](#)

BF Cockburn - Journal of Electronic Testing, 1994 - Springer

... Tutorial on Semiconductor **Memory Testing*** ... Editor: E Mazumder Abstract. This article
is a tutorial introduction to the field of semiconductor **memory testing**. ...

Cited by 30 - Related Articles - Web Search - BL Direct

[Badbit counter for memory testing - all 2 versions »](#)

JP Busack, GM Johnson, RR Clem... - US Patent 4,942,576, 1990 - Google Patents

... L r ti -^ b zI ZI ZI ZI r 5 5 4 i j CD Ü_ 4,942,576 I2 BADBIT COUNTER FOR MEMORY
TESTING ... 2a, to combinations; use of level-triggering versus **edge**-trig- ...

Cited by 20 - Related Articles - Web Search

[Edge programmable timing signal generator - all 3 versions »](#)

JR Shaw - US Patent 4,675,546, 1987 - Google Patents

... complete **edge** programmability for accommodating incremen- tally adjustable variable
pulse widths. The timing cir- cuit is particularly useful in **memory testing** ...

Cited by 31 - Related Articles - Web Search

[A gate-array-based 666 MHz VLSI test system - all 3 versions »](#)

S Kikuchi, Y Hayashi, T Suga, J Saitou, M Kaneko, ... - Test Conference, 1995. Proceedings., International, 1995 -
ieeexplore.ieee.org

... 38411s with a minimum resolution of 12.5s. The system also integrates a shared pattern
generator dedicated for the **memory testing**, which provides ... k DRV Edge 1 ...

Cited by 29 - Related Articles - Web Search - BL Direct

[Dependence of explicit and implicit memory on hypnotic state in trauma patients - all 4 versions »](#)

GH Lubke, C Kerssens, H Phaf, PS Sebel - Anesthesiology, 1999 - anesthesiology.org

... not be obtained reliably before surgery and was obtained subsequently before **memory**
testing. ... the ground electrode approximately 2 cm to the right **edge** of the ...

Cited by 101 - Related Articles - Web Search - BL Direct

[Testing embedded-core-based system chips - all 17 versions »](#)

Y Zorian, EJ Marinissen, S Dey - Computer, 1999 - doi.ieeecomputersociety.org

... test pattern sets, despite the amount of functionality knowl- **edge** or sophisticated ...
patterns, such as the regular patterns for **memory testing** [3] functional ...

Cited by 388 - Related Articles - Web Search - BL Direct

[Microprocessor based testing for core-based system on chip - all 6 versions »](#)

CA Papachristou, F Martin, M Nourani - Design Automation Conference, 1999. Proceedings. 36th, 1999 - ieeexplore.ieee.org

... **Testing** the microprocessor and the test memory is not the focus of our work. ... an **edge**
corresponds to the interconnects between ports or the bypass possibilities ...

Cited by 55 - Related Articles - Web Search - BL Direct

[Semiconductor memory testing apparatus - all 6 versions »](#)

S Sato - US Patent 5,790,559, 1998 - Google Patents

... 5,790,559 Aug. 4, 1998 [54] SEMICONDUCTOR **MEMORY TESTING APPARATUS** [75] Inventor:
Shinya Sato, Tokyo, Japan [73] Assignee: Advantest Corporation, Tokyo, Japan ...

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